TRUETIME

Model 560-5181-2
DIGITAL PRIMARY-SECONDARY SWITCH/DRIVER

SECTION ONE

1 FUNCTIONAL DESCRIPTION

1.1 PURPOSE OF EQUIPMENT

The TrueTime 560-5181-2 is configured to provide the user six digital outputs. The card provides output buffers that can be set for RS-422 100 Ohm operation or single ended TTL 50 Ohm operation (switch selectable). The six outputs (or output pairs in the case of RS-422) connect through the backplane connector and are delivered to external cables via the I/O card installed in the rear slot directly behind the 560-5181-2 card.

RS-422 NOTE: Output drive capability is switch-selectable for RS-422 100 Ohm or TTL 50 Ohm. The TTL setting provides enhanced drive capability, but allows the short circuit current to exceed the RS-422 specification. The output mode, single-ended or differential, is determined by the type of I/O card that is installed and the on-card switch setting.

The signal source for the card is one of the timing signals that is distributed via INPUT 1 through INPUT 8 on the Model 56000 backplane. The card is configured at installation by DIP switches to select the signal that will be the Primary and Secondary input.

The Primary and Secondary inputs are monitored for activity. The activity on both inputs is compared to the Delay switch time-out setting (user settable DIP switch SW3) which operates as a watch dog timer. If activity on either the Primary or the Secondary inputs exceeds the delay switch time-out setting, that input is considered bad. NOTE: An input may be considered bad if the minimum input voltage level is not met.

The 560-5181-2 card can operate without a Fault Monitor CPU card installed in the system. In a system without CPU card, the 560-5181-2 card will automatically switch to the Secondary input source when the following conditions are met:

1. The Secondary input is good (activity time-out not exceeded).
2. The Primary input is bad (activity time-out exceeded).

The card will not switch to the Secondary input source if it has been detected bad. The card will switch back to the Primary input signal source only after the Primary input has been qualified good (good for 1 to 2 minutes). This feature restores the card to normal operation automatically.

When a Fault Monitor CPU card is installed in the system, the 560-5181-2 card is monitored and can also be controlled by the CPU card. In addition to the 560-5181-2 on-card automatic Primary to Secondary switch-over, the CPU card also provides Primary to

Secondary input switching when the CPU detects a Primary Status Input fault. The CPU control provides what is called a "Bank Switch" meaning that all cards in the system will switch from the Primary to the Secondary signal source and will stay on the Secondary input until the user commands a switch to Primary via the CPU card. The "Bank Switch" allows timing signal inputs on all cards installed in the system to come from one source. The CPU also has the ability (under user control) to force the use of either the Primary or Secondary inputs.

1.2 FAULT LINE TRANSCEIVER FUNCTION

This is a serial half-duplex signaling operation between the 560-5181-2 card and the Fault Monitor CPU via the active-low FAULT signal line. The Fault Monitor CPU sends control and switching information to the 560-5181-2 assembly serially. The 560-5181-2 assembly provides status information serially to the Fault Monitor CPU.

1.3 PRIMARY/ SECONDARY SIGNAL SELECT FUNCTIONS

If the 560-5181-2 is operating using the Primary input signal and it detects inactivity on this input, the 560-5181-2 card will automatically or, under Fault Monitor CPU control, switch to the Secondary input signal. If the 560-5181-2 card is operating in a system with a Fault Monitor CPU card and the 560-5181-2 card has switched to the Secondary input source, the 560-5181-2 card will NOT switch back to the Primary input unless commanded by the user via the Fault Monitor CPU.

1.4 PHYSICAL SPECIFICATIONS

Dimensions:	0.8"w X 3.94"h X 8.66"d (2 cm X 10 cm X 22 cm)
Weight:	Approximately ½ pound (¼ kg)

1.5 ENVIRONMENTAL SPECIFICATIONS

Operating Temp:	0° to +50°C
Storage Temp:	-40° to +85°C
Humidity:	Up to 95% relative, non-condensing
Cooling Mode:	Convection
Altitude:	10,000 ft. ASL

1.6 POWER REQUIREMENTS

Voltage:	18-72 VDC
Power:	4 W (outputs A through F driving 50 ohm loads)

1.7 FUNCTIONAL SPECIFICATIONS

1.7.1 INPUT 1 THROUGH 8

Logic Input Levels:

Low:	-5V < Vin < 1.2V
High:	1.8V < Vin < 5.0V
Impedance:	>20k ohms
Frequency:	DC to 1 MPPS

1.7.2 TTL OUTPUTS (SWITCH SELECTABLE)

Quantity:	6
Signal Type:	TTL-level
Amplitude:	2.8 Vpk into 50 ohms
Signal Delay:	< 60 ns

1.7.3 RS-422 OUTPUTS (SWITCH SELECTABLE)

Quantity:	6 pairs
Signal Type:	Differential, centered at 2.5 VDC
Amplitude:	2.8 Vpp into 100 ohms
Signal Delay:	< 60 ns
Output Drive Compliance:	MIL-STD-188-114A TYPE II BALANCED RS-422-A

1.7.4 DRC CARD COMPATIBILITY

Location:	Slots 1-17 with compatible I/O card in rear slot.
Compatibility:	See Card Compatibility Matrix.

SECTION TWO

2 INSTALLATION AND OPERATION

2.1 HOT SWAPPING

All cards, input cables and output cables are hot swappable. It is not necessary to remove chassis power during insertion or removal. Hot swapping and reference-source changes are abrupt, the effects difficult to characterize; however, the system is designed to protect against permanent effects and minimize temporary effects of these events.

Typically, adjacent-card hot swapping has a negligible effect on the Digital output card. The effect of redundant power supply switch-over is also negligible.

2.2 REMOVAL AND INSTALLATION

CAUTION: Individual components on this card are sensitive to static discharge. Use proper static discharge procedures during removal and installation.

Refer to CARD COMPATIBILITY section prior to installing new card.

To remove card, loosen the captive retaining hardware at the top and bottom of the assembly, then firmly pull on the handle (or on any connector on rear panel adapter cards) at the bottom of the card. Slide the card free of the frame. Refer to the SETUP section for any required switch settings; or, set them identically to the card being replaced. Reinstall the card in the frame by fitting it into the card guides at the top and bottom of the frame and sliding it in slowly, avoiding contact between bottom side of card and adjacent card front panel, until it mates with the connector. Seat card firmly to avoid contact bounce. Secure the retaining screws at the top and bottom of the card assembly.

2.3 SETUP

The setup of the 560-5181-2 digital output card involves selection of the following DIP switches:

1. 560-5181-2 required settings (SW4 & SW7)
2. Primary input signal switch (SW5)
3. Secondary input signal switch (SW6)
4. Primary input enable switch (SW1)
5. Secondary input enable switch (SW2)
6. Delay switch (activity time-out) (SW3)
7. Delay switch (output faults) (SW3)
8. RS-422 / TTL switch (SW7)

2.3.1 560-5181-2 REQUIRED SETTINGS (SW4 & SW7)

SW4 and SW7 MUST be set as follows:
SW4 switches 1 through 8 = OFF
SW7 switches 1 through 7 = ON

2.3.2 PRIMARY INPUT SOURCE SWITCH (SW5)

Set one SW5 switch to the ON position. The SW5 switch number (1 through 8) corresponds to INPUT 1 through INPUT 8 signals that are distributed on the Model 56000 backplane.

2.3.3 SECONDARY INPUT SOURCE SWITCH (SW6)

Set one SW6 switch to the ON position. The SW6 switch number (1 through 8) corresponds to INPUT 1 through INPUT 8 signals that are distributed on the Model 56000 backplane.

2.3.4 PRIMARY INPUT ENABLE SWITCH (SW1)

This switch MUST be set to a binary representation of the SW5 setting, the Primary input signal switch. This switch is also read by the Fault Monitor CPU card which can provide status information to the user.

PRIMARY INPUT	SW1-1	SW1-2	SW1-3	SW1-4
INHIBIT	OFF	OFF	OFF	OFF
INPUT 1	ON	OFF	OFF	OFF
INPUT 2	OFF	ON	OFF	OFF
INPUT 3	ON	ON	OFF	OFF
INPUT 4	OFF	OFF	ON	OFF
INPUT 5	ON	OFF	ON	OFF
INPUT 6	OFF	ON	ON	OFF
INPUT 7	ON	ON	ON	OFF
INPUT 8	OFF	OFF	OFF	ON

This switch is also used to disable the Primary input. If SW1 switches 1 through 4 are OFF, the card will inhibit operation and fault reporting of the Primary input.

2.3.5 SECONDARY INPUT ENABLE SWITCH (SW2)

This switch MUST be set to a binary representation of the SW6 setting, the Secondary input signal switch. This switch is also read by the Fault Monitor CPU card which can provide status information to the user.

SECONDARY INPUT	SW2-1	SW2-2	SW2-3	SW2-4
INHIBIT	OFF	OFF	OFF	OFF
INPUT 1	ON	OFF	OFF	OFF
INPUT 2	OFF	ON	OFF	OFF
INPUT 3	ON	ON	OFF	OFF
INPUT 4	OFF	OFF	ON	OFF
INPUT 5	ON	OFF	ON	OFF
INPUT 6	OFF	ON	ON	OFF
INPUT 7	ON	ON	ON	OFF
INPUT 8	OFF	OFF	OFF	ON

This switch is also used to disable the Secondary input. If SW2 switches 1 through 4 are OFF, the card will inhibit operation and fault reporting of the Secondary input.

2.3.6 DELAY SWITCH (Activity Time-Out SW3 Switches 1, 2, & 3)

SW3 switches 1 through 3 are used to set the input activity time-out delay. The user should set the delay for a time-out value that is the closest to but longer than the period of the input signal. This will provide fault detection in the shortest amount of time (Primary to Secondary switch-over time is minimized).

Example Setting: If the input signal is 1 kPPS (1 millisecond period), the appropriate setting would be SW3-1 ON, SW3-2 OFF, SW3-3 OFF -- (2.048 millisecond time-out).

DELAY (TIME-OUT)	SW3-1	SW3-2	SW3-3
204.8 microseconds	OFF	OFF	OFF
2.048 milliseconds	ON	OFF	OFF
20.48 milliseconds	OFF	ON	OFF
204.8 milliseconds	ON	ON	OFF
2.048 seconds	OFF	OFF	ON
20.48 seconds	ON	OFF	ON
122.88 seconds	OFF	ON	ON
Infinite	ON	ON	ON

If infinite delay has been selected, Primary and Secondary input fault detection is disabled.

2.3.7 DELAY SWITCH (Output Fault Detection SW3-4)

SW3 switch 4 is used to enable or disable output fault detection. If the switch is ON, output fault reporting is disabled. The front panel output fault status LEDs are disabled (OFF) and output fault reporting to the CPU will cease.

2.3.8 RS-422 / TTL SWITCH (SW7-8)

SW7 switch 8 is the RS-422 / TTL mode control switch.

DIGITAL MODE	SW7-8
RS-422	OFF
TTL	ON

2.4 FAULT STATUS INDICATIONS

All LED indicators activate briefly following hot-insertion or power-up. The following paragraphs describe operation during steady-state conditions.

2.4.1 P/S FAULT INDICATOR

P/S = Primary/Secondary. The P/S indicator provides a visual indication of Primary and Secondary signal loss. If the Primary and the Secondary inputs are lost, the P/S LED will blink at a once per second rate (approx.). A solid ON P/S LED indicates a local power supply failure.

2.4.2 OUT FAULT INDICATORS

The OUT A through OUT F fault indicators activate when the associated drivers have failed. Note that the detector is designed to detect failed drivers and, typically, will not detect a shorted output.

2.4.3 INIT. FAULT INDICATOR

This is an on-card fault indicator which is not externally visible; although it can be seen by installing the card next to an empty slot. It indicates a failure of the card to initialize properly during power-up. Activation of this LED is accompanied by activation of all of the front panel indicators. Occasionally, this fault is caused by a temporary condition related to the cycling of power and can be cleared by a power or hot swap cycle. If this is unsuccessful, the card is defective.

2.4.4 DETAILED FAULT STATUS VIA CPU

The Fault Monitor CPU has access to detailed 560-5181-2 card status. This status is available via the Fault Monitor CPU serial port. When it is presented in a 2-byte format, with individual bit definitions as follows:

The Verbose report displays the Fault status. In this context, a reported fault indicates a problem. The Machine report, when used, reports the current status (settings) of the switches and faults in hexadecimal characters. Together, they pinpoint problems and help the technician view the switch settings on the cards without removing them.

2.4.5 VERBOSE REPORTS

The following is an example of a Fault Monitor CPU report in Verbose mode:

```
TrueTime 56000 Site 01
Automatic Reports Enabled
Periodic Reports Disabled
Primary Inputs Selected REFA No REFB No REFC Off PRI OK SEC OK TER Off

1. Undefined        OK          Undefined     OK
2. Undefined        OK          Undefined     OK
3. 5181-2    LOCAL OSC FAULT 0407 Undefined OK
4. Undefined        OK          Undefined     OK
```

The above sample tells you that:
Automatic reports are enabled and Periodic reports are disabled. Primary inputs REF A and REF B are not bussing AUX REF. REF C is off. Primary and Secondary status inputs OK, Tertiary is OFF.

Numbers 1-4 are slots (not all slots are shown in the example). Slots 1,2, and 4 are undefined (empty) and functional (OK).

Slot 3 is read as follows:
5181-2 is the abbreviation of the 560-5181-2 card. The fault reading is 0407.

2.4.6 MACHINE REPORTS

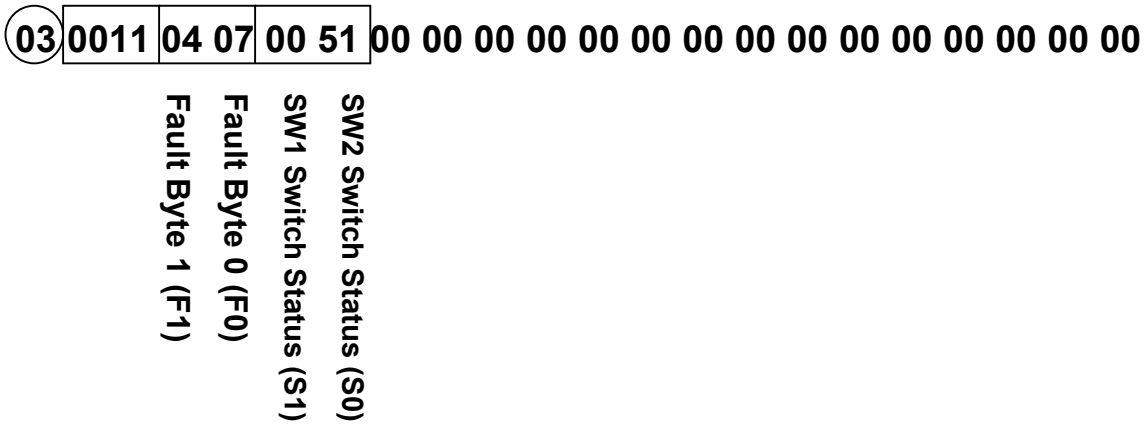
The Fault Monitor CPU has another serial output mode called machine report mode. This mode is usually used with a computer program to interrogate the 56000 system status.
The machine report mode displays hexadecimal (HEX) characters like the verbose mode report.

The following is an example of a Fault Monitor CPU report in Machine Mode:

```
TrueTime 56000 Site 01
AR1
PR10
P A1 B1 Co P1 S1 To
01 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
02 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
03 00 11 04 07 0051 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
04 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
(card slots 05 through 14 HEX not shown)

04  Fault Status (F1)      00  SW1 Switch Status (S1)
07  Fault Status (F2)      51  SW2 Switch Status (S0)
```

Example from card slot 3 :



Slot 3 shows that the Fault status is 0407 (F1, F0). The Status report read-out is 0051(S1, S0).

2.4.7 REPORT CONVERSIONS

This section deals with how to read and convert the Fault and Status read-outs using various tables and binary conversions. To decipher a Fault Status report, use Fig. A.
For Status reports (S1, S0) use Fig. B.

Fig. A

Spare	Spare	Spare	Spare	Pri. Source	Sec. Input Inactive*	Pri. Input Inactive*	Power Cycled	Undefined	Undefined*	Outpur Fault F*	Outpur Fault E*	Outpur Fault D*	Outpur Fault C*	Outpur Fault B*	Outpur Fault A*
8	**4**	**2**	**1**	**8**	**4**	**2**	**1**	**8**	**4**	**2**	**1**	**8**	**4**	**2**	**1**
2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0
0	*0*	*0*	*0*	*0*	*1*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*1*	*1*	*1*

Upper Byte High Nibble **0**

Upper Byte Low Nibble **4**

Lower Byte High Nibble **0**

Lower Byte Low Nibble **7**

Fault Status F1 Report

Fault Status F0 Report

Key:

Above each 8,4,2,1 is the corresponding fault for that bit. For instance, above the 8 bit in the Upper byte/Low nibble reads Rub. Lockmon, which is the fault .

Shaded area
Informational only. The upper row: Bit value hex weights (8,4,2,1) The Lower row corresponds to the hex weight above. For instance, a readout of 7 equals 111 in binary and 4+2+1 hex weight. Each section of 8,4,2,1 is a nibble of either an Upper or Lower byte and separated for easy recognition. Each nibble = 4 bits and each byte = 8 bits. "04" is the F1 report, "07" the F0 report.

Non-shaded area
This area is used according with the report read-out after a report is converted to binary. The 0407 is an example from a report.

Always read the report from Upper (High) byte to Lower (Low) Byte
* Latched Fault Bit -- Reset Via Fault Monitor CPU.

Always read the report from Upper (High) byte to Lower (Low) Byte.

Status (S1, S0) Conversion Table **FIG. B**

STATUS REG 0	Bit	Bit Value	Switch	
Low	0	1	Pri Input Enable SW1-1	
Nibble	1	2	Pri Input Enable SW1-2	**1**
Low	2	4	Pri Input Enable SW1-3	
Byte	3	8	Pri Input Enable SW1-4	
High	4	1	Sec Input Enable SW2-1	
Nibble	5	2	Sec Input Enable SW2-2	**5**
Low	6	4	Sec Input Enable SW2-3	
Byte	7	8	Sec Input Enable SW2-4	
STATUS REG 1				
Low	0	1	Delay SW3-1	
Nibble	1	2	Delay SW3-2	**0**
High	2	4	Delay SW3-3	
Byte	3	8	Output Faults OFF	
High	4	1	Always 1 (Analog)	
Nibble	5	2	Always 0	
High	6	4	Not Defined	**0**
Byte	7	8	Not Defined	

Notes: The settings listed under the Switch column are HIGH or ON. For instance, frequency has SW 1-1 and SW 1-2. If SW 1-1 is ON, SW 1-2 is presumed to be OFF (although there is no specific mention of this). For switches, a 1 = ON, 0 = OFF.

BINARY CONVERSION TABLE

Decimal	Displayed in report as	Binary
0	0	0

1	1	1
2	2	10
3	3	11
4	4	100
5	5	101
6	6	110
7	7	111
8	8	1000
9	9	1001
10	A	1010
11	B	1011
12	C	1100
13	D	1101
14	E	1110
15	F	1111

Binary:
1 = Fault/Switch On
0 = No Fault/Switch Off

Use the Binary Conversion table to convert a read-out from the monitor to binary. For instance, if the report read-out was 3C15, this would be:

11\1100\1\101 in binary.

USING THE FAULT STATUS REPORT (F0,F1)

The hex weight (fault importance) has been assigned 8, 4, 2, 1. Beneath each number is the corresponding fault. Use Fig. A. The report example read 0407. The 0 is high byte/high nibble, the 4, high byte/low nibble, the 0, low byte/high nibble and 7, low byte/low nibble. Each nibble falls under a section on Fig. A. high to low or left to right.

Look at Fig. A.. Below this is a sample read-out. This read-out would appear on the monitor when a Verbose report is requested. In the example, there are no faults in the upper byte/high nibble or in the lower byte/high nibble because both are zero (0). In the upper byte/low nibble, a 4 is reported. Looking directly above this, a 4 bit is easily spotted. The fault is Secondary Input Inactive. However, In the lower byte/low nibble a 7 is reported. There is no 7 listed, only a 1, 2, 4, 8. Use the Binary Conversion table to determine the faults.

Seven (7) is converted to 111 in Binary. In Binary, a 1 = fault and 0 = no fault. Read 111 from right (low bit) to left (high bit) using the lower byte/low nibble group. The first three (from low bit to high bit) are 1's, indicating there is a fault with the Output Faults A, B and C.

Note that the hex weight assigned totals to 7 (4+2+1). If the 7 had been a 6, in binary this is 110. Reading from low bit to high bit, the 1's (i.e., faults) fall under hex weight 4 and 2, which equals a hex weight of 6. Of course, glancing at the lower byte/low nibble, you can quickly see (without converting to binary) that under 4 and 2 (i.e., 6) are the Output C and Output B that are in fault.

Each of the four nibbles is grouped by category for easy visual identification of an offending fault. Each nibble has 15 possible fault combinations. All faults are asserted as a logic 1. The faults are latched on the Oscillator card and must be cleared by the 560-5179-1 Fault Monitor CPU “CL” command.

USING THE STATUS REPORT (S1, S0)

The method used for reading the Fault report is the same when reading the Status report. Refer to Fig. B.

Using the read-out, 0051, but because the table is different, the 0 is located at the high byte(8) of S1. The rest of the numbers follow upward towards the low byte and ending in Status 0. In this case, the 5 falls in the low byte section of Status 0(high nibble\low byte). The 5 is converted to binary, or 101 This indicates that the Secondary Input Enable SW2-1 and SW2-3 are active.

Sec Input Enable SW2-1	1
Sec Input Enable SW2-2	0
Sec Input Enable SW2-3	1

.

The 7 falls in the low nibble\low byte section of Status 0. Since 7 is not listed, we must convert it to binary, or 111. This indicates that Pri Input Enable SW1-1, SW1-2 and SW1-3 are active.

Pri Input Enable SW1-1	1
Pri Input Enable SW1-2	1
Pri Input Enable SW1-3	1

1 = Active, 0 = Not active.

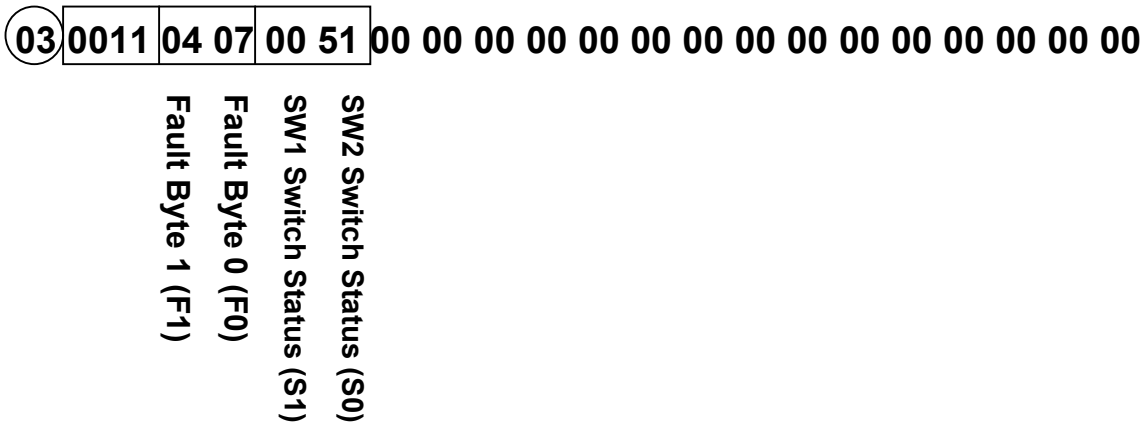
QUICK REFERENCE SHEET FOR READING FAULT AND STATUS REPORTS

1. Run a report. This is a portion of a sample Machine report.

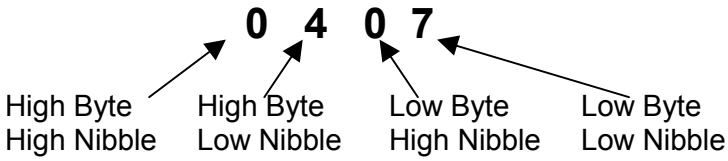
TrueTime 56000 Site 01
AR1
PR10
P A1 B1 Co P1 S1 To
01 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
02 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
03 0011 04 07 0051 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
04 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
(card slots 05 through 14 HEX not shown)

0407 is the Fault Status read-out
0051 is the Status read-out report

04 = Fault Status 1 (F1) report
07 = Fault Status 0 (F0) report
B0 = Status 1 (S1) report
51 = Status 0 (S0) report



What's in a number?



2. When required, convert Decimal to Binary using the Binary Conversion Table.

BINARY CONVERSION TABLE

Decimal	Displayed in report as	Binary
0	0	0
1	1	1
2	2	10
3	3	11
4	4	100
5	5	101
6	6	110
7	7	111
8	8	1000
9	9	1001
10	A	1010
11	B	1011
12	C	1100
13	D	1101
14	E	1110
15	F	1111

Binary:
1 = Fault/On/Active
0 = No Fault/Off/Not Active

SECTION THREE

3 THEORY OF OPERATION

3.1 GENERAL INFORMATION

This section contains a detailed description of the circuits in the 560-5181-2 Digital Output card. Use these descriptions in conjunction with the drawings in SECTION FOUR.

3.2 HARDWARE DESCRIPTION

The 560-5181-2 Digital Output card incorporates Primary and Secondary signal input source switches, a DC-to-DC Converter, six output drivers (six driver pairs in the case of RS-422), Input and Output fault-detection circuitry and 7 Fault Indicators.

3.3 DETAILED DESCRIPTION

Reference drawing 560-5181.

3.3.1 PRIMARY AND SECONDARY INPUTS (Sheet 6)

SW5 is the Primary Input select switch. One of the eight switches should be in the ON position. This switch directs the signal on backplane INPUT 1 through INPUT 8 to a voltage comparator. SW6 is the Secondary Input select switch. One of the eight switches should be in the ON position. This switch directs the signal on backplane INPUT 1 through INPUT 8 to a voltage comparator. The signals from the Primary and Secondary inputs are compared to a fixed voltage reference level with these comparators. NOTE: The input voltage level on the Primary and Secondary inputs must meet the minimum input voltage specifications or the input activity detection circuitry will indicate a loss of signal.

The output of the Primary and Secondary comparators connect to a Field Programmable Gate Array (FPGA) which monitors the inputs for activity. If both the Primary and Secondary inputs are detected bad, the front panel P/S fault status LED will blink at a once per second rate. This indicates that the Digital output card does not have a viable input signal source.

3.3.2 DIGITAL OUTPUTS (Sheet 5)

The output from the FPGA called “DIGITAL” is either the Primary or the Secondary signal source. The DIGITAL signal from the FPGA connects to two quad RS-422 which are the only drivers enabled in the RS-422 output mode. When the output mode is switched to TTL, SW7-8 ON, three more RS-422 drivers are enabled which are connected in parallel with the first two. The six non-complimentary outputs (A through F) are connected through Digital output switch SW7 to the backplane connector P1. The

RS-422 complimentary outputs (/A through /F) connect directly to the backplane connector P1.

3.3.3 POWER SUPPLY (Sheet 7)

The DC-to-DC Converter converts 48 VDC backplane power to local ±5 VDC power. It is fully-isolated from the backplane power and referenced to signal GND on the Digital output card. Backplane power is supplied via a Polyswitch fuse device, diode and Pi-section L-C filter. The poly-fuse protects the backplane power bus from internal DC-to-DC shorts. The diode and L-C filter serve a triple purpose. During live-insertion, the high-current inductor minimizes in-rush current to the DC-to-DC being inserted; and, the diode and capacitor serve to hold up the local voltage at the input to each currently-installed DC-to-DC. During steady-state conditions, the L-C filter minimizes switching noise coupled back into the backplane power bus. During live-extraction, the 0.1 uF capacitor absorbs the inductive-kick of the opened circuit, minimizing contact-arcing. The -5 VDC side of the supply is artificially loaded, providing a minimum load to improve output voltage regulation. The power-up reset generator, assures that RESET is active while the +5 VDC supply is between 1 and 4.5 VDC. This guarantees proper configuration of the Xilinx FPGA during hot swapping and power-up.

3.3.4 FPGA (Sheet 4)

The Field Programmable Gate Array (FPGA) is the interface between the Digital output card and the CPU (if installed). The FPGA provides the timing and control signals for the Digital output card in both local and CPU operating modes.

3.3.5 FAULT DETECTION (Sheets 4 & 6)

There are two categories of fault detection: Input signal faults and Output driver faults. Both use a combination of discrete components and Xilinx FPGA logic to perform the detection task.

Input signal faults are described in paragraph 3.3.1 “Primary & Secondary Inputs”. In the TTL mode, The output driver fault detector consists of a 1 of 8 analog multiplexer that samples the 6 digital outputs (DRIVOUT A through DRIVOUT F) under the control of the FPGA. In the RS-422 mode of operation, two 1 of 8 analog multiplexers are used to sample the twelve output signals (DRIVOUT A through DRIVOUT F and /DRIVOUT A through /DRIVOUT F).

The multiplexer(s) switch from output to output at a rate determined by the Delay switch (SW3) setting. The output from the multiplexer(s) connects to a voltage comparator which compares the card’s digital outputs to a fixed voltage reference level.

The output from the voltage comparator connects to the FPGA which operates internal watchdog timers that monitor activity on the six (or twelve) digital output signals. The watchdog timer time-out is based on the Delay switch setting (SW3). If the watchdog timer on a given output times out, the FPGA recognizes this as an output signal fault and activates the appropriate front panel LED fault indicator.

3.3.6 BACKPLANE FAULT OUTPUT

Inside the FPGA, all faults are combined to form a composite fault signal which is used to drive the Fault line to the Fault Monitor CPU. Fault-signal active indicates status-bit true. (Note that FAULT signal is active-low on the backplane.) Refer to manual section 2.4.4 for detailed information on fault reporting.

3.3.7 FAULT INDICATORS (Sheet 7)

The INIT. FAULT indicator is driven by the FPGA Initialization-done signal. It activates during initialization, and remains active if initialization does not complete. This is an extremely unusual occurrence.

The P/S FAULT indicator is powered directly from the backplane 48 VDC power buss and is controlled via an opto-isolator to maintain 48 VDC isolation. If local 5 VDC power is lost, the P/S indicator will be ON. The P/S indicator is held off by the Primary/Secondary input fault detection logic. When either of the input signal sources are viable, the indicator will be OFF. When both Primary and Secondary inputs are detected bad, the P/S FAULT indicator will blink ON and OFF.

The OUT fault indicators are controlled directly by the fault detection logic. NOTE: In RS-422 mode, OUT A through F LEDs indicate when either a non-complimented or complimented output fault condition exists.

SECTION FOUR

4. DETAILED DRAWINGS

4.1	560-5181	DETAILED DRAWINGS
4.2	560-5181-2	BILL OF MATERIALS